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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/264,085	03/08/1999	YOUSSEF ABDELILAH	RA9-98-074	2597

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EXAMINER	
KUMAR, PANKAJ	
ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 10/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No. 09/264,085	Applicant(s) ABDELILAH ET AL.	
	Examiner Pankaj Kumar	Art Unit 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,3,5-14,16-22,24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28 and 29* is/are allowed.

6)☒ Claim(s) *1, 2, 3, 6, 7, 8, 9, 11-14, 16-17, 19-22, 24, 25, 26, 27, 30* is/are rejected.

7)☒ Claim(s) *5,10 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. DETAILED ACTION

2. Response to Arguments

3. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

4. Response to Amendment

5. Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

7. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 20 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claims 20 and 30 recite the limitations "logic", "first logic" and "second logic". It is not clear whether the different places where "logic" is used pertains to "first logic", "second logic", or various independent logics. Since "first logic" and "second logic" are numerically noted, all of the logics should also be preceded by numerically notation.

10. Since claim 20 is rejected, claims 21, 22, 24, 25, 26 and 27 are also rejected.

11. Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

13. A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in

the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1, 2, 3, 9, 11-14, 16-17, 19-22, 25, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orban US pat. no. 6,337,999 in view of Serfaty US pat. no. 5,293,401.

15. Regarding claim 1, what Orban shows is a receiver (Orban fig. 2) for demodulating a data signal transmitted from a digital source (Orban col. 2 lines 26-27 “digital medium”) at a network sampling rate that is synchronized with a network clock (inherent since data is being sampled), comprising:

16. a two-stage interpolator (Orban fig. 2: 200,201), responsive to digital samples of the data signal, that generates interpolated digital samples in response thereto, the digital samples having a first local sample rate that is synchronized with a local clock and the interpolated digital samples having a second local sample rate that is synchronized with the network clock (inherent for there to be two different clocks since there are multiple interpolations and we want to save power), wherein the two-stage interpolator comprises:

17. a polyphase interpolator (Orban fig. 2: 200, 201 are polyphase since the input is comprised of multiple frequencies and since phase is directly proportional to frequency, the interpolators are working on polyphase signals), responsive to the digital samples of the data signal, that generates first and second estimates for each of the digital samples of the data signal; and

18. a linear interpolator (Orban col. 3 line 64 to col. 4 line 7: FIR filter is polyphase and linear; if the filter was not linear, then the interpolation would not be linear; since the filter is linear and Orban does not mention quadratic interpolator or something similar, it is inherent for Orban’s interpolator to be linear; also Orban mentions upsampling and this is inherently linear),

responsive to the first and second estimates, that generates the interpolated digital samples. What Orban does not show is an adaptive fractionally spaced decision feedback equalizer, responsive to the interpolated digital samples, that generates equalized digital samples at the network sampling rate in synchronization with the network clock; and a slicer (Orban fig. 2: 400, 401), responsive to the equalized digital samples, that generates detected symbols therefrom corresponding to data from the data signal. What Serfaty shows is a DFE (Serfaty fig. 4: 39) after interpolation (Serfaty fig. 4: 36) within the same field of endeavor. What Orban shows is a slicer (Orban fig. 2: 400, 401) that generates detected symbols corresponding to data from the data signal; however, since there is no DFE in Orban, this slicer is not responsive to equalized digital samples. It would have been obvious to one skilled in the art at the time of the invention to modify Orban to include a DFE of Serfaty after the interpolations since they are both in the same field of endeavor and doing so would result is a better performing system.

19. Regarding claim 2, Orban with Serfaty show a receiver as recited in Claim 1, wherein the adaptive fractionally spaced decision feedback equalizer has a tap spacing given by pT/q where T is a modulation interval associated with the network sampling rate and p and q are integers (it is inherent for taps to be spaced at a multiple of the higher sampling rate since the data is at the high rate when it enters the DFE).

20. Regarding claim 3, Orban with Serfaty show a receiver as recited in Claim 1, further comprising a clock synchronizer (inherent) responsive to the detected symbols and generating a

sampling index signal (Serfaty fig. 4: 31-decide if counter K=Nth sample in frame), the two-stage interpolator being responsive to the sampling index signal; (Serfaty fig. 4: 36).

21. Claim 4 has been cancelled.

22. Regarding claim 9, a receiver as recited in Claim 1, further comprising:

23. means for identifying a signaling alphabet used by the slicer to generate the detected symbols (Orban fig. 1: 60 shows a clipper – one letter in the alphabet).

24. Regarding claim 11, a receiver as recited in Claim 1, wherein the detected symbols are pulse code modulation (PCM) codewords (inherent for modulated digital signals to be PCM).

25. Regarding claim 12, Orban shows a method for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock (inherent), comprising the steps of:

26. sampling the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock (Orban sampling for fig. 2: 200);

27. interpolating the digital samples to produce first and second estimates for each of the digital samples (inherent if I and Q samples existed in Orban) using a polyphase interpolator (Orban: polyphase since the input is comprised of multiple frequencies and since phase is directly proportional to frequency, the interpolators are working on polyphase signals);

28. interpolating the first and second estimates to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock (Orban sampling for fig. 2: 201) using a linear interpolator (Orban col. 3 line 64 to col. 4 line 7: FIR filter is polyphase and linear; if the filter was not linear, then the interpolation would not be linear; since the filter is linear and Orban does not mention quadratic interpolator or something similar, it is inherent for Orban's interpolator to be linear; also Orban mentions upsampling and this is inherently linear);

29. What Orban does not show is equalization. What Serfaty shows (as discussed above) is equalizing the interpolated digital samples to produce equalized digital samples; and decoding the equalized digital samples to generate detected symbols therefrom.

30. Regarding claim 13. A method as recited in Claim 12, wherein the equalizing step comprises the step of using an adaptive fractionally spaced decision feedback equalizer that has a tap spacing given by pTlq where T is a modulation interval associated with the network sampling rate and p and q are integers to produce the equalized digital samples (discussed above).

31. Regarding claim 14. A method as recited in Claim 12, further comprising the step of: maintaining the synchronization between the second local sample rate (Serfaty fig. 4: K) and the network clock (Serfaty fig. 4: N) via a sampling index signal (Serfaty fig. 4: N/2).

32. Claim 15 has been cancelled.

33. Regarding claim 16, a method as recited in Claim 12, further comprising the steps of: coupling a transmitter to the receiver with an echo canceller; receiving at an input of the echo canceller transmit symbols from the transmitter that have a third local sample rate that is synchronized with the local clock; and generating at an output of the echo canceller echo cancellation samples at the first local sample rate in synchronization with the local clock (discussed above).

34. Regarding claim 17, a method as recited in Claim 12, further comprising the step of identifying a signaling alphabet for use in the decoding step to generate the detected symbols (discussed above in claim 9).

35. Regarding claim 19, a method as recited in Claim 12, wherein the detected symbols are pulse code modulation (PCM) codewords (discussed above in claim 11).

36. Claims 20-22, 25, 27 are rejected over Orban in view of Serfaty based on the reasoning in regards to other claims above. Orban and Serfaty show logic diagrams that may be coded.

37. Claim 23 is cancelled.

38. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Orban in view of Hodgkiss US pat. no. 5,293,401. Orban and Hodgkiss all show logic diagrams that may be

coded. Hodgkiss shows equalizer and echo canceller. The remainder of the discussion combining these two references is discussed in other paragraphs.

39. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orban and Serfaty as applied to claim 1 above, and further in view of Hodgkiss US pat. no. 5,293,401.

40. Regarding claim 6, Orban with Serfaty show a receiver as recited in Claim 1. What Orban with Serfaty does not show is an echo canceller. Hodgkiss shows an echo canceller (Hodgkiss fig. 3 "echo canceller") that couples a transmitter to the receiver, the echo canceller being responsive to transmit symbols from the transmitter that have a third local sample rate (Hodgkiss col. 1 lines 55 to col. 2 line 7: transmitter clock signal used for echo canceller is distinguished from first series clock signal and second series clock signal) that is synchronized with the local clock and generating echo cancellation samples in response thereto at the first local sample rate in synchronization with the local clock (Hodgkiss col. 2 line 6: "time intervals determined by received signal components"). Since Hodgkiss is in the same field of endeavor as Orban and Serfaty, it would have been obvious to one skilled in the art at the time of the invention to modify Orban with Serfaty as discussed in claim 1 and further with Hodgkiss by adding an echo canceller. One would be motivated to do so for a more efficient system.

41. Regarding claim 7, Orban with Serfaty with Hodgkiss show a receiver as recited in Claim 6, further comprising an adder that combines the echo cancellation samples with the digital samples of the data signal (Orban fig. 2: 480).

42. Regarding claim 8, Orban with Serfaty with Hodgkiss show a receiver as recited in Claim 6, wherein the echo canceller comprises an adaptive digital filter (Hodgkiss figs.10-12, "automatic gain control"; col.5 line 55 "adapting the echo canceller process"), responsive to the transmit symbols from the transmitter (Hodgkiss col. 5 lines 45-46 "echoes of the transmitted signal"), that generates echo cancellation samples at the first local sample rate in synchronization with the receiver clock (Hodgkiss col. 1 lines 59-64; fig. 3 echo cancel is after a/d; col. 2 lines 5-7 "second sequence .. at time intervals determined by received signal ..."), which are complementary to a portion in each of the digital samples of the data signal that can be attributed to an echo signal from the transmitter.

43. Allowable Subject Matter

44. Claim 26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

45. Claims 5, 10 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

46. Claims 28 and 29 are allowed.

47. As per claim 28, what Orban shows is a receiver (Orban fig. 2) for demodulating a data signal transmitted from a digital source (Orban col. 2 lines 26-27 "digital medium") at a network

sampling rate that is synchronized with a network clock (inherent since data is being sampled), comprising:

48. a two-stage interpolator (Orban fig. 2: 200,201), responsive to digital samples of the data signal, that generates interpolated digital samples in response thereto, the digital samples having a first local sample rate that is synchronized with a local clock and the interpolated digital samples having a second local sample rate that is synchronized with the network clock (inherent for there to be two different clocks since there are multiple interpolations and we want to save power). What Orban does not show is an adaptive fractionally spaced decision feedback equalizer, responsive to the interpolated digital samples, that generates equalized digital samples at the network sampling rate in synchronization with the network clock; and a slicer (Orban fig. 2: 400, 401), responsive to the equalized digital samples, that generates detected symbols therefrom corresponding to data from the data signal. What Serfaty shows is a decision feedback equalizer (Serfaty fig. 4: 39) after interpolation (Serfaty fig. 4: 36) within the same field of endeavor. What Orban shows is a slicer (Orban fig. 2: 400, 401) that generates detected symbols corresponding to data from the data signal; however, since there is no DFE in Orban, this slicer is not responsive to equalized digital samples. It would have been obvious to one skilled in the art at the time of the invention to modify Orban to include a DFE of Serfaty after the interpolations since they are both in the same field of endeavor and doing so would result is a better performing system; means for identifying a signaling alphabet used by the slicer to generate the detected symbols (Orban fig. 1: 60 shows a clipper – one letter in the alphabet); means for establishing a plurality of alphabetic thresholds (Yoshida USPN 4792964 "The output of multiplier 3 is coupled to a decision circuit 4 which converts it to a signal having discrete

amplitude levels by comparison with multiple decision thresholds."); ***means for computing an average value for the equalized digital samples corresponding to a particular alphabet threshold (not in the cited references)***.

49. As per claim 29, Orban shows a method for demodulating, in a receiver, a data signal transmitted from a digital source at a network sampling rate that is synchronized with a network clock (inherent), comprising the steps of:

50. sampling the data signal to produce digital samples at a first local sample rate that is synchronized with a local clock (Orban sampling for fig. 2: 200);

51. interpolating the digital samples to produce first and second estimates for each of the digital samples (inherent if I and Q samples existed in Orban);

52. interpolating the first and second estimates to produce interpolated digital samples having a second local sample rate that is synchronized with the network clock (Orban sampling for fig. 2: 201)

53. What Orban does not show is equalization. What Serfaty shows (as discussed above) is equalizing the interpolated digital samples to produce equalized digital samples; and decoding the equalized digital samples to generate detected symbols therefrom.

54. identifying a signaling alphabet ... comprising the steps of establishing a plurality of alphabetic thresholds (Yoshida USPN 4792964 "The output of multiplier 3 is coupled to a decision circuit 4 which converts it to a signal having discrete amplitude levels by comparison with multiple decision thresholds."); ***computing an average value for the equalized digital samples corresponding to a particular alphabet threshold (not in the cited references)*** ...

55. None of the references cited discuss computing an average value for the equalized digital samples corresponding to a particular alphabet threshold as it pertains to the objected claims.

56. None of the references cited discuss the polyphase interpolator being responsive to the first integer and the linear interpolator being responsive to the second integer

57. Conclusion

58. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

59. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

60. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Monday through Thursday after 8AM to after 6:30PM.

61. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

62. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

63.

64.

65. PK
66. October 8, 2002

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 10/10/02